IFW

A-8753W
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Gerald J. BANKS

Appln. No.: 10/742,890 Group Art Unit: 2824

Filed: December 23, 2003 Examiner: H. Nguyen

For: MEMORY APPARATUS INCLUDING PROGRAMMABLE NON-VOLATILE MULTI-BIT MEMORY CELL, AND APPARATUS AND METHOD FOR DEMARCATING MEMORY STATES OF CELL

Allowed: May 18, 2004

Confirmation No.: 7102

* * *

REQUEST FOR ACKNOWLEDGEMENT OF INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Mail Stop Issue Fee

Sir:

An Information Disclosure Statement was filed on May 17, 2004, prior to the allowance of the subject application. A copy of the Information Disclosure Statement and the date-stamped postcard receipt are attached.

Applicant respectfully requests that the Examiner confirm consideration of the Information Disclosure Statement by returning an endorsed copy of the Form PTO-1449.

Respectfully submitted,

By: _____
Mitchell W. Shapiro
Reg. No. 31,568

MWS:sjk

Miles & Stockbridge P.C.
1751 Pinnacle Drive
Suite 500
McLean, Virginia 22102-3833
(703) 903-9000

June 1, 2004

(16)

Applicant: Gerald J. BANKS
Appln No.: 10/742,890
Filed On: December 23, 2003
For: MEMORY APPARATUS INCLUDING PROGRAMMABLE NON-VOLATILE MULTI-BIT MEMORY CELL, AND APPARATUS AND METHOD FOR DEMARCATING MEMORY STATES OF CELL

T3055-907736US02
A-8753W

Attached: Information Disclosure Statement w/ Form PTO-1449.

RECEIVED IN U.S. PATENT AND TRADEMARK OFFICE ON:

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Appln. No.: 10/742,890 Group Art Unit: 2818

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* * *

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant wishes to make of record the documents cited in predecessor Application Nos. 10/188,835 filed July 5, 2002, 09/893,545 filed June 29, 2001, 09/733,937 filed December 12, 2000, 09/493,139 filed January 28, 2000, 09/411,315 filed October 4, 1999, 08/975,919 filed November 21, 1997, and 08/410,200 filed February 27, 1995, whether cited by Applicant or by the Patent Office. The documents are listed on the attached Form-1449 and include all citations through AT on sheet 27 of the List. The

remaining document on sheet 27 is the patent which issued on parent Application No. 10/188,835.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees that may be required by this paper and to credit any overpayment to that Account.

Respectfully submitted,

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LIST OF DOCUMENTS CITED BY APPLICANT

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	AA	5,200,920	04/06/93	Norman et al.	365	185	
	AB	Re 32,401	04/14/87	Belistein, Jr. et al	365	182	
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	AL	56-114199	09/08/81	Japan			No
	AM	61-239497	10/24/86	Japan			No
	AN	61-239498	10/24/86	Japan			No
	AO	62-24499	02/02/87	Japan			No
	AP	1-159895	06/22/89	Japan			No
	AQ						

OTHER (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	Torelli, Guido et al., "An Improved Method for Programming a Word-Erasable EEPROM", Alta Frequenza - Scientific Review in Electronics, Vol. LII, No. 6, Pages 487-494 (1983).
	AS	Yoshikawa, Kuniyoshi et al., "An Asymmetrical Lightly-Doped Source (ALDS) Cell for Virtual Ground High Density EPROMs", IEEE International Electron Devices Meeting, 1988, Pages 432-435.

Examiner	Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	AA	4,417,325	11/22/83	Harari	365	185	
	AB	4,448,400	5/15/84	Harari	365	185	
	AC	4,612,629	9/16/86	Harari	365	185	
	AD	5,043,940	8/27/91	Harari	365	168	
	AE	5,163,021	11/10/92	Mehrotra et al.	365	185	
	AF	5,168,465	12/1/92	Harari	257	320	
	AG	5,198,380	3/30/93	Harari	437	43	
	AH	5,200,959	4/6/93	Gross et al.	371	21.6	
	AI	5,268,318	12/7/93	Harari	437	43	
	AJ	5,268,319	12/7/93	Harari	437	43	
	AK	5,268,870	12/7/93	Harari	365	218	
	AL	5,272,669	12/21/93	Samachisa et al.	365	185	
	AM	5,293,560	3/8/94	Harari	365	185	
	AN	5,313,421	5/17/94	Guterman et al.	365	185	
	AO	5,422,842	6/6/95	Cernea et al.	365	185	
	AP	5,428,621	6/27/95	Mehrotra et al.	371	21.4	
	AQ	5,430,859	7/4/95	Norman et al.	395	425	
	AR	5,434,825	7/18/95	Harari	365	185	
	AS	5,495,442	2/27/96	Cernea et al.	365	185.03	
	AT	5,544,118	8/6/96	Harari	365	218	
	AU	5,554,553	9/10/96	Harari	437	43	
	AV	5,568,439	10/22/96	Harari	365	218	
	AW	5,583,812	12/10/96	Harari	365	185.33	
	AX	5,642,312	6/24/97	Harari	365	185.33	
	AY	5,657,332	8/12/97	Auclair et al.	371	40.11	
	AZ	5,659,550	8/19/97	Mehrotra et al.	371	21.4	

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Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	BA	5,712,180	1/27/98	Guterman et al.	437	43	
	BB	5,712,819	1/27/98	Harari	365	185.29	
	BC	5,776,810	7/7/98	Guterman et al.	438	258	
	BD	5,806,070	9/8/98	Norman et al.	711	103	
	BE	4,661,929	4/285/87	Aoki et al.	365	189	
	BF	4,701,884	10/20/87	Aoki et al.	365	189	
	BG	4,709,350	11/24/87	Nakagome et al.	365	45	
	BH	5,014,242	5/7/91	Akimoto et al.	365	63	
	BI	5,299,165	3/29/94	Kimura et al.	365	210	
	BJ	5,307,304	4/26/94	Saito et al.	365	145	
	BK	5,802,553	9/1/98	Robinson et al.	711	103	
	BL	5,801,991	9/1/98	Keeney et al.	365	185.23	
	BM	5,796,667	8/18/98	Sweha et al.	365	207	
	BN	5,781,472	7/14/98	Sweha et al.	365	185.11	
	BO	5,754,566	5/19/98	Christopherson et al.	371	40.18	
	BP	5,748,546	5/5/98	Bauer et al.	365	210	
	BQ	5,671,388	9/23/97	Hasbun	395	430	
	BR	5,574,879	11/12/96	Wells et al.	395	427	
	BS	5,566,125	10/15/96	Fazio et al.	365	45	
	BT	5,563,828	10/8/96	Hasbun et al.	365	185.33	
	BU	5,553,020	9/3/96	Keeney et al.	365	185.19	
	BV	5,546,042	8/13/96	Tedrow et al.	327	538	
	BW	5,497,354	3/5/96	Sweha et al.	365	230.06	
	BX	5,487,033,	1/23/96	Keeney et al.	365	185.19	
	BY	5,438,546	8/1/95	Ishac et al.	365	200	

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Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	AA	4,192,014	03/04/80	Craycraft	365	104	
	AB	4,357,685	11/02/82	Daniele et al.	365	189	
	AC	4,964,079	10/16/90	Devin	365	168	
	AD	5,172,338	12/15/92	Mehrotra et al.	365	185	
	AE	5,262,984	11/16/93	Noguchi et al.	365	185	
	AF	3,801,965	04/02/74	Keller et al.	340	173R	
	AG	4,004,159	01/18/77	Rai et al.	307	238	
	AH	4,054,864	10/18/77	Audaire et al.	340	173R	
	AI	4,090,258	05/16/78	Cricchi	365	184	
	AJ	4,122,541	10/24/78	Uchida	365	154	
	AK	4,139,910	02/13/79	Anantha et al.	365	183	

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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	AL	WO82/02276	07/08/82	WIPO			
	AM	WO82/02976	09/02/82	WIPO			
	AN	WO90/01984	03/08/90	WIPO			
	AO	2 630 574	10/27/89	France			Abstract
	AP	0 390 404	10/03/90	Europe			
	AQ	0 725 403	08/07/96	EPO			

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	M. Bauer et al., *A Multilevel-Cell 32Mb Flash Memory*, 1995 IEEE International Solid-State Circuits Conference, Session 7, Paper TA7.7.
	AS	John A. Bayliss et al., *The Interface Processor for the 32b Computer*, 1981 IEEE International Solid-State Circuits Conference, February 1981, at 116-117.

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U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	AA*	4,149,270	04/10/79	Cricchi et al.	365	222	
	AB*	4,181,980	01/01/80	McCoy	365	45	
	AC*	4,272,830	06/09/81	Moench	365	45	
	AD*	4,287,570	09/01/81	Stark	365	104	
	AE*	4,300,210	11/10/81	Chakravarti et al.	365	45	
	AF*	4,306,300	12/15/81	Terman et al.	365	45	
	AG*	4,327,424	04/27/82	Wu	365	104	
	AH*	4,388,702	06/14/83	Sheppard	365	104	
	AI*	4,415,992	11/15/83	Adlhoch	365	94	
	AJ*	4,449,203	05/15/84	Adlhoch	365	104	
	AK*	4,462,088	07/24/84	Giuliani et al.	365	105	

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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
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	AR*	Christoph Bleiker & Hans Melchior, *A Four-State EEPROM Using Floating-Gate Memory Cells*, IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 3, June 1987, at 260-263.
	AS*	Raymond A. Heald & David A. Hodges, *Multilevel Random-Access Memory Using One Transistor Per Cell*, IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 4, August 1976, at 519-528.

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Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	AA^	4,495,602	01/22/85	Sheppard	365	104	
	AB^	4,503,518	03/05/85	Iwahashi	365	104	
	AC^	4,558,241	12/10/85	Suzuki et al.	307	530	
	AD^	4,578,777	03/25/86	Fang et al.	365	184	
	AE^	4,586,163	04/29/86	Koike	365	104	
	AF^	4,627,027	12/02/86	Rai et al.	365	45	
	AG^	4,653,023	03/24/87	Suzuki et al.	365	104	
	AH^	4,661,929	04/28/87	Aoki et al.	365	189	
	AI^	4,709,350	11/24/87	Nakagome et al.	365	45	
	AJ^	4,733,394	03/22/88	Giebel	371	21	
	AK^	4,771,404	09/13/88	Mano et al.	365	189	

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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	AL^						
	AM^						
	AN^						
	AO^						
	AP^						
	AQ^						

OTHER (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR^	David A. Rich, *A Survey of Multivalued Memories*, IEEE Transactions on Computers, Vol. C-35, No. 2, February 1986, at 99-106.
	AS^	R.S. Withers et al., *Nonvolatile Analog Memory in MNOS Capacitors*, IEEE Electron Device Letters, Vol. EDL-1, No. 3, March 1980, at 42-45.

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Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	AA#	4,799,195	01/17/89	Iwahashi et al.	365	185	
	AB#	4,847,808	07/11/89	Kobatake	364	104	
	AC#	4,853,892	08/01/89	Hori	365	49	
	AD#	4,890,259	12/26/89	Simko	365	45	
	AE#	4,914,631	04/03/90	Johnson et al.	365	189.11	
	AF#	4,989,179	01/29/91	Simko	365	45	
	AG#	5,021,999	06/04/91	Kohda et al.	365	168	
	AH#	5,043,940	08/27/91	Harari	365	168	
	AI#	5,095,344	03/10/92	Harari	357	23.5	
	AJ#	5,163,021	11/10/92	Mehrotra et al.	365	185	
	AK#	5,258,958	11/02/93	Iwahashi et al.	365	210	

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	AL#						
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	AN#						
	AO#						
	AP#						
	AQ#						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR#	"Mid-Level Current Generator Circuit", IBM Technical Disclosure Bulletin, Vol. 33, No. 1B, 1 June 1990, pp. 386-388.
	AS#	
	AT#	

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	AA'	5,268,870	12/07/93	Harari	365	218	
	AB'	5,293,560	03/08/94	Harari	365	185	
	AC'	5,321,655	06/14/94	Iwahashi et al.	365	200	
	AD'	5,351,210	09/27/94	Saito	365	189.01	
	AE'	5,422,845	06/06/95	Ong	365	185	
	AF'	5,432,735	07/11/95	Parks et al.	365	168	
	AG'	5,434,825	07/18/95	Harari	365	185	
	AH'	5,440,505	08/08/95	Fazio et al.	365	45	
	AI'	5,444,656	08/22/95	Bauer et al.	365	189.01	
	AJ'	5,450,363	09/12/95	Christopherson et al.	365	205	
	AK'	5,457,650	10/10/95	Sugiura et al.	365	184	

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	AA~	5,469,384	11/21/95	Lacey	365	185.13	
	AB~	5,475,693	12/12/95	Christopherson et al.	371	10.2	
	AC~	5,485,422	01/16/96	Bauer et al.	365	168	
	AD~	5,497,119	03/05/96	Tedrow et al.	327	540	
	AE~	5,506,813	04/09/96	Mochizuki et al.	365	230.03	
	AF~	5,508,958	04/16/96	Fazio et al.	365	185.19	
	AG~	5,515,317	05/07/96	Wells et al.	395	427	
	AH~	5,523,972	06/04/96	Rashid et al.	365	185.22	
	AI~	5,539,690	07/23/96	Talreja et al.	365	185.22	
	AJ~	5,541,886	07/30/96	Hasbun	365	230.01	
	AK~	5,544,118	08/06/96	Harari	365	218	

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	AC❖	5,583,812	12/10/96	Harari	365	185.33	
	AD❖	5,594,691	01/14/97	Bashir	365	189.09	
	AE❖	5,596,527	01/21/97	Tomioka et al.	365	185.20	
	AF❖	3,660,819	05/02/72	Frohman-Bentchkowsky	317	235R	
	AG❖	5,295,255	03/15/94	Malecek et al.	395	425	
	AH❖						
	AI❖						
	AJ❖						
	AK❖						

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	AA	3,755,721	8/28/73	Frohman-Bentchkowksky	317	235R	
	AB	5,021,999	6/4/91	Kohda et al.	365	168	
	AC	4,903,236	2/20/90	Nakayama et al.	365	185	
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	AH						
	AI						
	AJ						
	AK						

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	AP						

OTHER (including author, title, date, pertinent pages, etc.)

	AQ	Bleiker, Christoph, and Melchior, Hans. "A Four-State EEPROM Using Floating-Gate Memory Cells." IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 3. (June 1987) : 460-463.
	AR	Intel Corporation. "2764A Advanced 64K (8K x 8) Production and UV Erasable PROMs." Memory Components Handbook. (October 1985) : 4.10-4.20.
	AS	Chi, Min-hwa, and Bergemont, Albert. "Multi-level Flash/EPROM Memories: New Self-convergent Programming Methods for Low-voltage Applications." 1995 Technical Digest-International Electron Devices Meeting. (1995) : 271-274.

Examiner	Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	BL						
	BM						
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OTHER (including author, title, date, pertinent pages, etc.)

	BQ	Aritome, Seiichi, et al. "A Novel Side-Wall Transfer-Transistor Cell (SWATT Cell) For Multi-Level NAND EEPROMs." 1995 Technical Digest-International Electron Devices Meeting. (1995) : 275-278.
	BR	Bauer, M., et al. "TA 7.7: A Multilevel-Cell 32Mb Flash Memory." 1995 IEEE International Solid-State Circuits Conference, 1995 Digest of Technical Papers. (1995) : 132-133.
	BS	Hemink, G.J., et al. "Fast and Accurate Programming Method for Multi-level NAND EEPROMs." 1995 Symposium on VLSI Technology Digest of Technical Papers. (1995) : 129-130.

Examiner	Date Considered

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U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	CL						
	CM						
	CN						
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OTHER (including author, title, pertinent pages, etc.)

	CQ	Takeuchi, Ken, et al. "A Double-Level-V_{th} Select Gate Array Architecture for Multi-Level NAND Flash Memories." 1995 Symposium on VLSI Circuits Digest of Technical Papers. (1995) : 69-70.
	CR	Gotou, Hiroshi. "New Operation Mode for Stacked-Gate Flash Memory Cell." IEEE Electron Device Letters, Vol. 16, No. 3. (March 1995) : 121-123.
	CS	Jung, Tae-Sung, et al. "TP 2.1: A 3.3V 128Mb Multi-Level NAND Flash Memory for Mass Storage Applications." 1996 IEEE International Solid-State Circuits Conference, 1996 Digest of Technical Papers. (1996) : 32-33.

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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	DL						
	DM						
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OTHER (including author, title, date, pertinent pages, etc.)

	DQ	Neale, Ron. "Will multi-level Flash memory be the way to the future?" Electronic Engineering (London), Vol. 68, No. 835. (July 1996): 3 pp.
	DR	Patton, Robert. "Flash makers taking conservative steps forward." Japanese Press Network. (November 1996) : 2 pp.
	DS	Ohkawa, Masayoshi, et al. "TP 2.3: A 98mm^2 3.3V 64Mb Flash Memory with FN-NOR Type 4-level Cell." 1996 IEEE International Solid-State Circuits Conference, 1996 Digest of Technical Papers. (1996) : 36-37.

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	EL						
	EM						
	EN						
	EO						
	EP						

OTHER (including author, title, date, pertinent pages, etc.)

	EQ	Montanari, D., et al. "Multi-Level Charge Storage in Source-Side Injection Flash EEPROM." 1996 IEEE International NonVolatile Memory Technology Conference. (1996) : 80-83.
	ER	Atwood, Greg, et al. "Intel StrataFlash Memory Technology Overview." Intel Technology Journal. (Fourth quarter 1997) : 1-8.
	ES	Fazio, Al, and Bauer, Mark. "Intel StrataFlash Memory Technology Development and Implementation." Intel Technology Journal. (Fourth quarter 1997) : 1-13.

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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	FL						
	FM						
	FN						
	FO						
	FP						

OTHER (including author, title, date, pertinent pages, etc.)

	FQ	Intel Corporation. "Intel StrataFlash Memory Technology." Intel Technical Paper. (September 1997) : 1-13.
	FR	Candelier, Ph., et al. "Hot Carrier Self Convergent Programming Method for Multi-Level Flash Cell Memory." 1997 35th Annual IEEE International Reliability Physics Symposium. (1997) : 104-109.
	FS	Intel Corporation. "Intel StrataFlash Memory Technology 32 and 64 Mbit." Intel Advance Information. (January 1998) : 1-53.

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	GL						
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	GP						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	GQ	Alberts, G.S., and Kotecha, H.N. "Multi-Bit Storage FET EAROM Cell." IBM Technical Disclosure Bulletin, Vol. 24, No. 7A. (December 1981) : 3311-3314.
	GR	Blyth, Trevor, et al. "TPM 11.7: A Non-Volatile Analog Storage Device Using EEPROM Technology." 1991 IEEE International Solid-State Circuits Conference, Digest of Technical Papers. (February 1991) : 192-193 and 315.
	GS	Hanyu, T., et al. "Functionally separated, multiple-valued content-addressable memory and its applications." IEE Proceedings-Circuits Devices Systems, Vol. 142, No. 3. (June 1995) : 165-172.

Examiner	Date Considered

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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	HL						
	HM						
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OTHER (including author, title, date, pertinent pages, etc.)

	HQ	English abstract of "Flash Memories-Interview with Intel Corporation Representative." Elektronik Praxis 30(10). (24 May 1995) : 26-30.
	HR	Tran, Hieu Van, et al. "FP 16.6: A 2.5V 256-Level Non-Volatile Analog Storage Device Using EEPROM Technology." 1996 IEEE International Solid-State Circuits Conference. (February 1996) : 270-271, 458, and 512.
	HS	Choi, Young-Joon, et al. "A High Speed Programming Scheme for Multi-Level NAND Flash Memory." 1996 Symposium on VLSI Circuits Digest of Technical Papers. (1996) : 170-171.

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	IL						
	IM						
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	IP						

OTHER (Including author, title, date, pertinent pages, etc.)

	IQ	Giridhar, Raghupathy V. "Flash Technology: Challenges and Opportunities." Japanese Journal of Applied Physics, Vol. 35 (1996), Part I, No. 12B, Review Papers. (December 1996) : 6347-6350.
	IR	Gill, Manzur. "Flash Memories: A Review." 1996 IEEE International NonVolatile Memory Technology Conference. (1996) : 142. Abstract provided only.
	IS	Calligaro, C., et al. "Technological and Design Constraints for Multilevel Flash Memories." 1996 IEEE International Conference on Electronic Circuits and Systems. (1996) : 1005-1008.

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	JL						
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OTHER (including author, title, date, pertinent pages, etc.)

	JQ	Eitan, Boaz, et al. "Multilevel Flash cells and their Trade-offs." 1996 IEEE International Electron Devices Meeting. (1996) : 169-172.
	JR	Yoshikawa, Kuniyoshi. "Impact of Cell Threshold Voltage Distribution in the Array of Flash Memories on Scaled and Multilevel Flash Cell Design." 1996 Symposium on VLSI Technology Digest of Technical Papers. (1996) : 240-241.
	JS	Hanyu, Takahiro, et al. "Non-Volatile One-Transistor-Cell CAM and Its Applications." Methodologies for the Conception, Design, and Applications of Intelligent Systems, Proceedings of IIZUKA. (October 1996) : 101-104.

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	KL						
	KM						
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	KP						

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	KQ	Calligaro, C., et al. "Mixed Sensing Architecture for 64Mbit 16-Level-Cell Non-Volatile Memories." 1996 IEEE Innovative Systems in Silicon Conference. (October 1996) : 133-140.
	KR	Hanyu, Takahiro, et al. "Design of a One-Transistor-Cell Multiple-Valued CAM." IEEE Journal of Solid-State Circuits, Brief Papers, Vol. 31, No. 11. (November 1996) : 1669-1674.
	KS	Kencke, D.L., et al. "A Sixteen Level Scheme Enabling 64Mbit Flash Memory Using 16Mbit Technology." 1996 International Electron Devices Meeting. (1996) : 937-939.

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FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	LL						
	LM						
	LN						
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OTHER (including author, title, date, pertinent pages, etc.)

	LQ	De Graaf, C., et al. "Feasibility of Multilevel Storage in Flash EEPROM Cells." Proceedings of the 25th European Solid State Device Research Conference. (September 1995) : 213-216.
	LR	Aritome, Seiichi, et al. "A Side-Wall Transfer-Transistor Cell (SWATT Cell) for Highly Reliable Multi-Level NAND EEPROM's." IEEE Transactions on Electron Devices, Vol. 44, No. 1. (January 1997) : 145-152.
	LS	Gotou, H. "An Experimental Confirmation of Automatic Threshold Voltage Convergence in a Flash Memory Using Alternating Word-Line Voltage Pulses." IEEE Electron Device Letters, Vol. 18, No. 10. (October 1997) : 503-505.

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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	ML						
	MM						
	MN						
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OTHER (including author, title, date, pertinent pages, etc.)

	MQ	Kim, H.S., et al. "Fast Parallel Programming of Multi-Level NAND Flash Memory Cells Using the Booster-Line Technology." 1997 Symposium on VLSI Technology Digest of Technical Papers. (1997) : 65-66.
	MR	Takeuchi, Ken, et al. "A Multi-Page Cell Architecture for High-Speed Programming Multi-Level NAND Flash Memories." 1997 Symposium on VLSI Circuits Digest of Technical Papers. (1997) : 67-68.
	MS	Choi, Jung Dal, et al. "A Triple Polysilicon Stacked Flash Memory Cell with Wordline Self-Boosting Programming." 1997 IEEE International Electron Devices Meeting. (1997) : 283-286.

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	NM						
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OTHER (including author, title, date, pertinent pages, etc.)

	NQ	Shen, Shih-Jye, et al. "Novel Self-Convergent Programming Scheme for Multi-Level P-Channel Flash Memory." 1997 IEEE International Electron Devices Meeting. (1997) : 287-290.
	NR	Otsuka, Nobuaki, and Horowitz, Mark A. "Circuit Techniques for 1.5-V Power Supply Flash Memory." IEEE Journal of Solid-State Circuits, Vol. 32, No. 8. (August 1997) : 1217-1230.
	NS	Hanyu, Takahiro, et al. "TP 2.5: 2-Transistor-Cell 4-Valued Universal-Literal CAM for a Cellular Logic Image Processor." 1997 IEEE International Solid-State Circuits Conference. (February 1997) : 46-47 and 362.

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	OL						
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OTHER (including author, title, date, pertinent pages, etc.)

	OQ	Eitan, Boaz. "Hot Carrier Effects in FLASH." Microelectronic Engineering, Vol. 36. (June 1997) : 277-284.
	OR	Montanari, Donato, et al. "Voltage Variant Source Side Injection for Multilevel Charge Storage in Flash EEPROM." IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A. Vol. 20, No. 2. (June 1997) : 196-202.
	OS	Calligaro, Cristiano, et al. "Comparative Analysis of Sensing Schemes for Multilevel Non-Volatile Memories." 1997 Proceedings of the Second Annual IEEE International Conference on Innovative Systems in Silicon. (October 1997) : 266-273.

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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	PL						
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OTHER (including author, title, date, pertinent pages, etc.)

	PQ	Lorenzini, Martino, et al. "A Dual Gate Flash EEPROM Cell with Two-Bit Storage Capacity." IEEE Transactions on Components, Packaging and Manufacturing Technology, Part A. Vol. 20, No. 2. (June 1997) : 182-189.
	PR	Bonner, Bruce. "New Flash Market Attracts SGS and Mitsubishi." Dataquest, The Semiconductor DQ Monday Report, Issue 8. (March 2, 1998). Dataquest Analysis provided only.
	PS	Donoghue, Bill, et al. "A 256K HCMOS ROM Using a Four-State Cell Approach." IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 2. (April 1985) : 598-602.

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	AA	4,809,224	02/28/89	Suzuki et al.	365	168	
	AB	5,218,569	06/08/93	Banks	365	189.01	
	AC	5,872,735	02/16/99	Banks	365	189.01	
	AD	6,002,614	12/14/99	Banks	365	189.01	
	AE	6,104,640	08/15/00	Banks	365	189.01	
	AF	6,011,716	01/04/00	Banks	365	185.03	
	AG	6,014,327	01/11/00	Banks	365	185.03	
	AH	6,118,692	09/12/00	Banks	365	185.03	
	AI	6,246,613	06/12/01	Banks	365	189.01	
	AJ	6,243,321	06/05/01	Banks	365	233	
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	AO	6,324,121	11/27/01	Banks	365	185.03	
	AP	6,327,189	12/04/01	Banks	365	189.01	
	AQ	6,404,675	06/11/02	Banks	365	185.03	
	AR	6,344,998	02/05/02	Banks	365	185.22	
	AS	6,434,050	08/13/02	Banks	365	185.2	
	AT	6,381,172	04/30/02	Banks	365	185.03	
	AU	6,714,455	03/30/04	Banks	419	27	

OTHER (including author, title, date, pertinent pages, etc.)

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